CLAIMS

What is claimed is:

1. An assembly, comprising:

an integrated circuit die having a substantially planar surface, a power supply conductor, a ground conductor and a signal conductor;

a package, the package housing the integrated circuit die and having an inside upper surface and a landing pad; and

a caposer having a first surface, a first conductive layer, a second conductive layer, and a second surface, wherein the first conductive layer and the second conductive layer are substantially planar and are parallel to one another, the first conductive layer being coupled to the power supply conductor, the second conductive layer being coupled to the ground conductor, the caposer having a through-hole that extends from the first surface, through the first and second conductive layers and to the second surface, wherein the signal conductor of the integrated circuit die is coupled to the landing pad through the through-hole without being coupled to the first conductive layer or the second conductive layer, wherein the first surface of the caposer is disposed adjacent to the substantially planar surface of the integrated circuit die, and wherein the second surface of the caposer is disposed adjacent to the inside upper surface of the package.

2. The assembly of claim 1, wherein the caposer further comprises a dielectric layer, the dielectric layer being disposed between the first conductive layer and the second conductive layer, and wherein the first conductive layer, the dielectric layer and the second conductive layer together constitute a bypass capacitor.

3. The assembly of claim 1, wherein the integrated circuit die further comprises a micro-bump, the micro-bump being coupled to the signal conductor, and wherein the micro-bump extends through the through-hole and contacts the landing pad.

4. The assembly of claim 3, wherein the integrated circuit die further comprises a plurality of micro-bumps disposed in a pattern on the substantially planar surface, and wherein the caposer has a plurality of through-holes, the plurality of through-holes of the caposer being disposed in a pattern that substantially matches the pattern of micro-bumps on the substantially planar surface.

5. The assembly of claim 1, wherein the integrated circuit die further comprises a micro-bump, the micro-bump being coupled to the signal conductor, and wherein the caposer further comprises a conductive via disposed in the through-hole, and wherein the signal conductor of the integrated circuit die is coupled at least in part by the conductive via to the landing pad of the package.

6. The assembly of claim 5, wherein the integrated circuit die further comprises a plurality of micro-bumps disposed in a pattern on the substantially planar surface, and wherein the caposer further comprises a plurality of conductive vias disposed in a pattern, each conductive via of the plurality of conductive vias extending from the first surface of the caposer to the second surface of the caposer, and wherein the pattern of conductive vias of the caposer substantially matches the pattern of micro-bumps of the integrated circuit die.

7. The assembly of claim 1, wherein the caposer further comprises a solder plug, at least a part of the solder plug being disposed in the through-hole such that the solder plug

extends from the first surface of the caposer to the second surface of the caposer.

8. The assembly of claim 7, wherein the through-hole has a volume, and wherein the solder plug includes a volume of solder that exceeds the volume of the through-hole.

9. The assembly of claim 7, wherein the solder plug extends beyond the first surface in a direction perpendicular to the first surface, and wherein the solder plug extends beyond the second surface in a second direction opposite the first direction.

10. The assembly of claim 1, wherein the caposer is less than 100 microns thick.

11. The assembly of claim 1, wherein the caposer includes no semiconductor material.

12. The assembly of claim 1, wherein the caposer includes no transistor and no PN junction.

13. The assembly of claim 1, wherein the caposer includes no logic element.

14. A method, comprising:

assembling a caposer, an integrated circuit die, and a package, wherein the integrated circuit die includes a signal conductor, and wherein the caposer includes a bypass capacitor and has a through-hole that extends through the caposer, the bypass capacitor having a first plate and a second plate, the signal conductor being coupled through the through-hole of the caposer to a landing pad on an inside upper surface of the package such that the signal conductor is not coupled to the first plate of the bypass capacitor and is not coupled to the second plate of the bypass capacitor.

15. The method of Claim 14, wherein the integrated circuit die further comprises a power supply conductor, and wherein the caposer, the integrated circuit die and the package are assembled such that the power supply conductor is coupled to the first plate of the bypass capacitor, further comprising:

drawing a current onto the integrated circuit die through the power supply conductor, wherein at least a portion of the current is supplied to the integrated circuit die from the bypass capacitor.

16. The method of Claim 14, wherein the integrated circuit die includes a plurality of micro-bumps, wherein the caposer includes a plurality of through-holes, and wherein said assembling is conducted such that each respective one of the micro-bumps of the integrated circuit die extends through a corresponding one of the through-holes of the caposer.

17. The method of Claim 14, wherein the integrated circuit die includes a plurality of micro-bumps, wherein the caposer includes a plurality of conductive vias, and wherein said assembling is conducted such that each respective one of the plurality of micro-bumps of the integrated circuit die contacts a corresponding one of the plurality of conductive vias of the caposer.

18. The method of Claim 14, wherein the integrated circuit die includes a plurality of lands, and wherein the caposer includes a plurality of solder plugs, and wherein the assembling is conducted such that each respective one of the plurality of lands of the integrated circuit die contacts a corresponding one of the plurality of solder plugs of the caposer.

19. A structure, comprising:

an integrated circuit die having a signal conductor;

an integrated circuit package housing the integrated circuit die, a landing pad being disposed on an inside surface of the integrated circuit package; and

means for supplying a bypass capacitor within the integrated circuit package such that the signal conductor of the integrated circuit die is coupled to the landing pad of the integrated circuit without being coupled to the bypass capacitor.

20. The structure of Claim 19, wherein the means is disposed between the integrated circuit die and the inside surface of the integrated circuit package, wherein the integrated circuit die has a power conductor, wherein the bypass capacitor has a first conductive plate and a second conductive plate, and wherein the power conductor is coupled to the first conductive plate.

21. A structure having a rectangular tile shape, a rectangular upper surface and rectangular bottom surface, the structure comprising:

a first conductive plate;

a second conductive plate disposed parallel to the first conductive plate; and

a dielectric layer disposed between the first conductive plate and the second conductive plate, wherein each through-hole of a plurality of through-holes extends through the structure from the rectangular upper surface, through the first conductive plate, through the dielectric layer, through the second conductive plate and to the rectangular bottom surface, wherein each of the through-holes has an inside surface, wherein neither the first conductive plate nor the second conductive plate extends to the inside surface of at least one of the through-holes, and wherein the tile-shaped structure is less than 100 microns thick.